## IN THE SPECIFICATION

3. The Examiner objected to the abstract because of a grammatical informality. Please amend the abstract in the manner noted below. The amendment is believed to introduce no new matter. The objection is believed overcome.

A method, apparatus and system for building a filter is disclosed. In a particular embodiment, the filter is a finite impulse response (FIR) filter and a compiler suitable for implementing the FIR filter is described. The compiler has an ~~includes~~ a filter coefficient generator suitably arranged to provide a first set of filter coefficients corresponding to the desired FIR filter spectral response and a filter spectral response analyzer coupled to the filter coefficient generator for providing an expected FIR filter spectral response based in part upon the first set of filter coefficients. The compiler also includes a filter resource estimator coupled to the filter spectral response simulator for estimating an implementation cost of the FIR filter based upon the second set of filter coefficients as well as a filter compiler unit coupled to the resource estimator arranged to compile a FIR filter implementation output file.

5. The Examiner objected to page 3, line 5, as "values" should read "value." Please amend the paragraph on page 3, lines 3-12 in the manner noted below. The amendment is believed to introduce no new matter. The objection is believed overcome.

Digital signal processors (DSPs) have a limited number of multiplier accumulators (MACs) which require many clock cycles to compute each output value ~~values~~ since the number of cycles is directly related to the order of the filter. Once a particular FIR filter design has been finalized, the FIR filter can take the form of a dedicated hardware solution which typically can achieve one output per clock cycle. However, by using a programmable integrated circuit, such as a programmable logic device (PLD) such as those manufactured by the Altera Corporation of San Jose CA, a fully parallel, pipelined FIR filter implemented, or "fitted", in a PLD and can operate at data rates above 100 million samples per second (MSPS), thereby making PLDs an ideal platform for high speed filtering applications.

6. The Examiner objected the phrase "input data rate/decimation factor." Please amend the paragraph on page 24, line 19 – page 25, line 12 in the manner noted below. The amendment is believed to introduce no new matter. The objection is believed overcome.

In those cases when it would be advantageous to optimize a decimating FIR filter using a serial filter, the FIR compiler is capable of building a decimating FIR filter by using a polyphase decomposition where each of the polyphases is a serial FIR filter. In this way, a single clock domain can be used for each serial filter as well as for the final adder. In order to accomplish this, the FIR compiler has developed the following clock rules. One such set of clock rules requires that in those cases where the input data width is less than or equal to the decimation factor, the clock rate is equal to the input data rate and the output data rate is equal to the input data rate divided by the decimation ~~rate/decimation~~ factor. In addition, the input data is then held for decimation factor clock cycles. In this way the decimation scheme switches through all polyphases at every clock cycle. However, in those cases where the input data width is greater than the decimation factor, the clock rate is set equal to a speed multiplication factor (SMF1) multiplied by the input data rate. In the described embodiment, SMF1 is the smallest integer such that SMF1 multiplied by the decimation factor is greater than or equal to the input data width. In addition, the output data rate is set equal to the (SMF1) multiplied by the input data rate divided by the decimation factor and the output data is then held for (SMF1) multiplied by the decimation factor clock cycles.